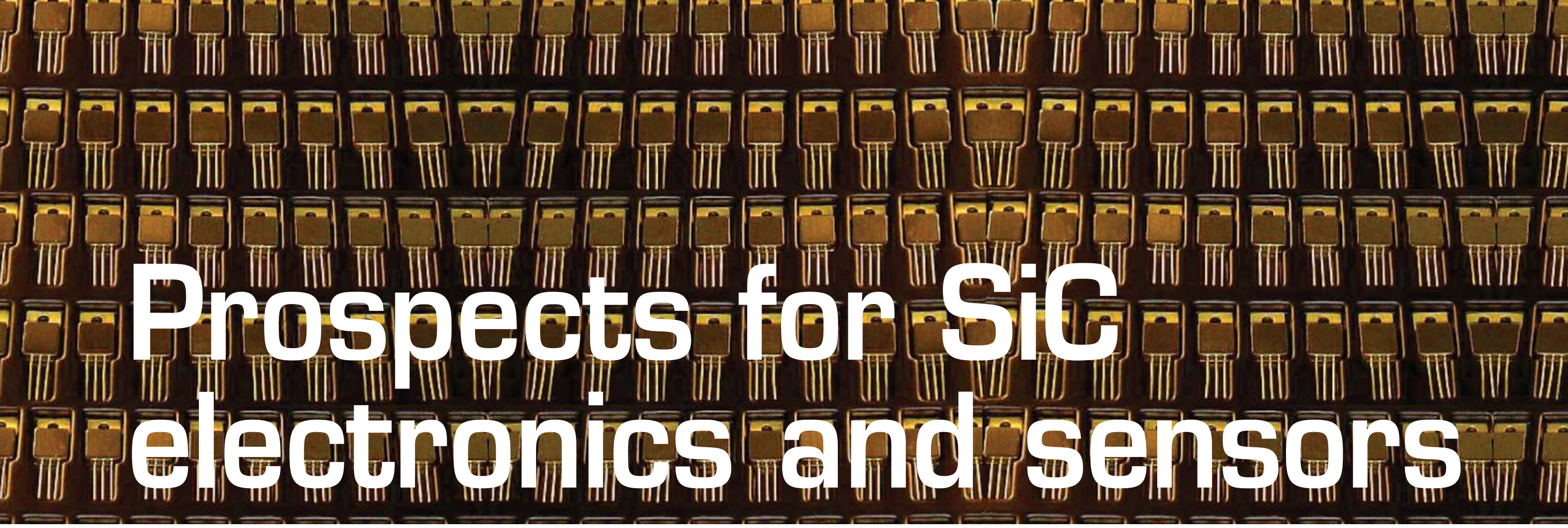

Prospects for SiC electronics and sensors

There has been substantial international research effort in the development of SiC electronics over the last ten years. With promising applications in power electronics, hostile-environment electronics, and sensors, there is considerable industrial interest in SiC as a material for electronics. However, issues relating to crystal growth and the difficulties of material processing have restricted SiC devices to relatively limited use to date. The eventual success of SiC as an electronic technology will depend on the close interplay of research in fundamental material science with progress in design of electronic devices and packaging. We review the current status of SiC electronics from a materials perspective – highlighting current difficulties and future opportunities for progress.

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The development of SiC technology over the last few years has been quite dramatic, with significant improvements in wafer growth technology, materials processing, electronic devices, and, increasingly, sensors. The underlying rationale for these investments in SiC technology is its excellent material properties, which derive in general from the high strength of the Si–C bond.

In fact, SiC exists in a large number of polytypes – different crystal structures built from the same Si–C subunit organized into a variety of stacking sequences[1]. Such polytypes are distinguished by the type of the crystal lattice (i.e. hexagonal, cubic, or rhombohedral) and the number of layers making up the repeat pattern, e.g. 4H-SiC has a hexagonal lattice with a four-layer repeat structure. There are over 100 of these polytypes known, but the majority of research and development has concentrated on three: 3C, 6H, and 4H. Of these, the 4H polytype is the most common for electronic devices because of its overall superior material properties, which drive investment in this area. The bandgap of 4H-SiC is 3.23 eV at room temperature (compared with 1.12 eV for Si). This dramatically reduces the number of electron-hole pairs formed from thermal activation across the bandgap and allows high-temperature operation of SiC electronic devices, including sensors[2]. The 3C-SiC polytype is more common for microelectromechanical systems (MEMS)-based sensors because it

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may be grown in polycrystalline form on Si wafers (thus reducing the overall wafer cost compared with pure SiC technology). Other material advantages for all forms of SiC include a high radiation and chemical tolerance, a high thermal conductivity (better than Cu), high hardness and Young's modulus (typically ~450 GPa compared with ~130 GPa for Si), and for some polytypes (notably 4H and 6H) a high critical electric field (in excess of 2 $MVcm^{-1}$)[1,2]. This combination of excellent electronic and mechanical properties offers many possibilities for using SiC as a material for a wide range of devices and sensors – particularly in applications featuring high temperatures or hostile environments. Such applications may include controlling electrical power distribution in aeroplanes, *in situ* monitoring of combustion processes (helping to make such processes more efficient and controlling unwanted emissions) or scientific applications (such as uncooled radiation detectors in new generations of spacecraft). This review discusses the use of SiC as a material for a range of different types of electronic devices and applications. We highlight key material advantages, summarize the current status of device processing, and provide a detailed discussion of potentially valuable applications. However, it is worth noting that the prospects for SiC are not all in the future – in fact, SiC Schottky diodes have been commercially available since 2001 and are now widely used in many practical applications.

General materials processing issues

SiC has a large number of different crystallographic forms or polytypes. For some years, 6H-SiC had the most developed growth technology on account of its relatively large volume usage as a substrate for GaN blue light-emitting diodes (LEDs), but this has now been matched or perhaps exceeded by the 4H polytype. The preferred material for many electronic applications is in fact 4H-SiC, which exhibits an on-axis mobility nearly ten times that of 6H-SiC[3]. At present, commercial 4H-SiC wafers are available up to 75 mm and 100 mm in diameter[4]. Substrates are available in both low resistivity (*n*- and *p*-type) and semi-insulating forms[5], although the moderate-to-high resistivity substrates desirable for high-voltage devices are not available. Devices are, therefore, typically fabricated on homoepitaxial layers, which are routinely grown to thicknesses of over 100 μm with doping densities as low as 10^{14} cm^{-3} using hot wall chemical vapor deposition (CVD)[6]. High-level carrier lifetimes for this material are typically of the order of several hundred nanoseconds making it suitable for the fabrication of bipolar devices with voltage blocking capabilities approaching 10 kV[7].

Historically, the major difficulty with SiC has been the presence in the substrates and epilayers of micropipes, which are essentially small holes (of diameter ~1 μm) running through the wafer from top to bottom. However, since material with essentially zero micropipe densities is now available (reduced from over 1000 cm^{-2} in just a few years)[5], indications are that SiC is adequate to fabricate devices several millimeters square with reasonable yield. The emphasis on defects is now switching from micropipes to closed-core screw dislocations, as there is a positive correlation between dislocation density and reduced breakdown voltages[8,9]. Indications are that a dislocation density of less than 10 cm^{-2} is desirable for the fabrication of power devices for high-temperature operation[9] (current values are typically ~10 000 cm^{-2} but decreasing rapidly). A further difficulty concerns the uniformity of epilayer doping and thickness across the wafer (typical results show a standard deviation of 4% on thickness and 8% on doping) and the uniformity of doping between runs (typically 40%)[5].

One of the principle benefits of SiC is that it oxidizes to form a stable surface layer of SiO_2, releasing CO_2 in the process. However, the detailed properties of that oxide and, in particular, the interface between SiC and SiO_x are significantly different from Si[10]. The oxidation rate is crystal-orientation dependent and is far slower on the Si face than the C face, with, in general, much better properties found for the oxide than on the Si face. Oxidation temperatures are normally ~1100°C and, unlike Si, a post-oxidation anneal in a hydrogen ambient is usually reported to have little effect at reducing interface state density[11]. Interface state densities on the 4H polytype rise very rapidly toward the conduction band edge, which has been ascribed to a carbon-related acceptor located just below the conduction band edge for 4H[12]. These defects have not been successfully removed by any standard surface treatment or post-oxidation anneal, but the effect can be reduced by nitrogen incorporation during oxide growth or post-oxidation anneal.

The breakdown and reliability properties of SiO_2 are crucial for all metal-oxide-semiconductor (MOS) devices, but unfortunately the situation is not as favorable as it is for Si. For simple MOS field-effect transistor (MOSFET) designs, the ratio of the dielectric constants of SiC and SiO_2 produces a surface electric field ~2.5 times higher in the oxide than in SiC[13]. Hence, to gain the full benefit of the ~2.5 $MVcm^{-1}$ breakdown field of SiC, the oxide must withstand 6.25 $MVcm^{-1}$, which is higher than is reliably usable, even on Si[2]. However, this can be mitigated by the use of more complex structures or by careful device design. High field stressing of oxides has shown that those grown in a wet ambient breakdown at lower fields than dry-grown oxides[14] and that extrapolated time-dependent dielectric-breakdown lifetimes of ten years can only be obtained on *n*-type at fields less than 5 $MVcm^{-1}$ at room temperature. Studies have shown that the lifetime of oxides drops rapidly at elevated temperatures[15], with a vulnerability to negative-bias-stress instability[16]. Electron injection into the oxide is more efficient than for Si because of the lower barrier and the induced defects are more stable[11]. In addition, the barrier for injection of holes is much lower than in Si, which is unfortunate since holes are particularly damaging to oxides[17].

The selective doping of a SiC wafer via ion implantation is of crucial importance for device fabrication and there have been extensive studies of ion implantation of a range of dopant atoms into SiC[18]. To anneal defects out of a wafer and to activate the dopant, it is essential to anneal the wafer at high temperatures post-implant.

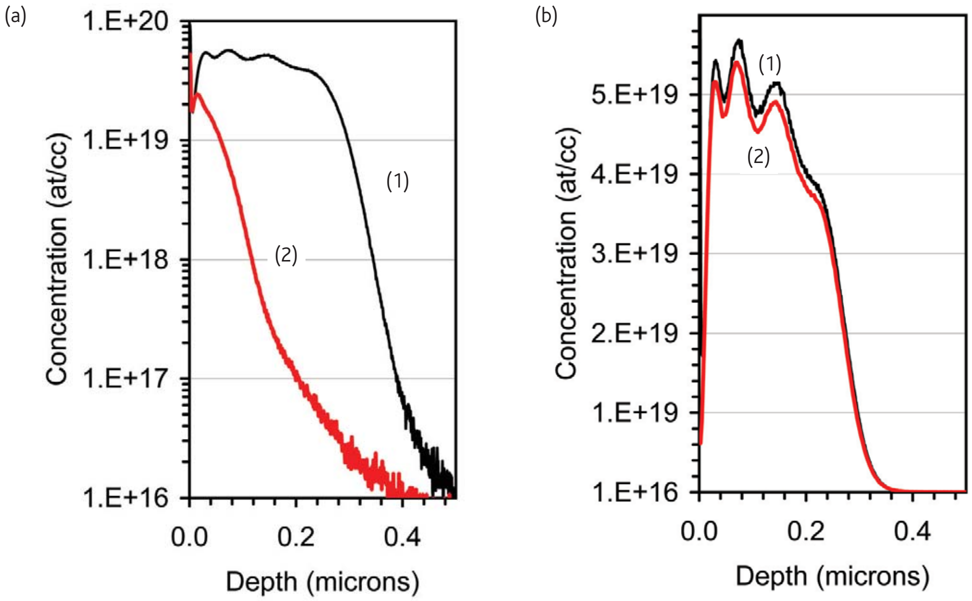

Fig. 1 Al distributions in 4H-SiC samples measured by secondary ion mass spectroscopy (SIMS) before (1) and after (2) annealing at 1600°C for 30 min without (a) and with (b) a graphite capping layer. Al is a p-type dopant in SiC but can diffuse heavily out of samples (as in (a)) if capping is not used.

This is typically carried out at temperatures as high as 1700°C and is technologically difficult because of the instability of the SiC surface at such temperatures. Si atoms sublime at temperatures above 1400°C, destroying the stoichiometry of the near-surface region and causing macro-step formation and introducing defects. This effect can be mitigated by using a Si over-pressure in the annealing furnace (typically introduced by using a silane atmosphere) or by capping the wafer with a robust material such as graphite (Fig. 1)[19,20].

SiC for power electronics

The outstanding physical properties of SiC[21] make it one of the materials best suited to the fabrication of high-power and high-temperature semiconductor devices[22]. As a result, substantial research efforts are being devoted toward fabricating most types of semiconductor device in SiC, although it is Schottky diode, junction field-effect transistor (JFET), MOSFET, and bipolar junction transistor (BJT) devices that attract most interest. Although significant progress has taken the place in the development of SiC MOSFETs, their introduction into high-power electronics is still limited by their low channel mobility, low reliability of the gate oxide, and threshold voltage instability[23,24]. Bipolar devices are perceived to be more suitable for very high voltage applications and so at present it is the unipolar JFET devices that are perhaps the most prominent (Fig. 2).

In recent years, a number of SiC power JFET designs have been developed. They include JFETs either with a lateral (LJFET)[25] or a vertical (VJFET)[26,27] current control channel above the drift region, as

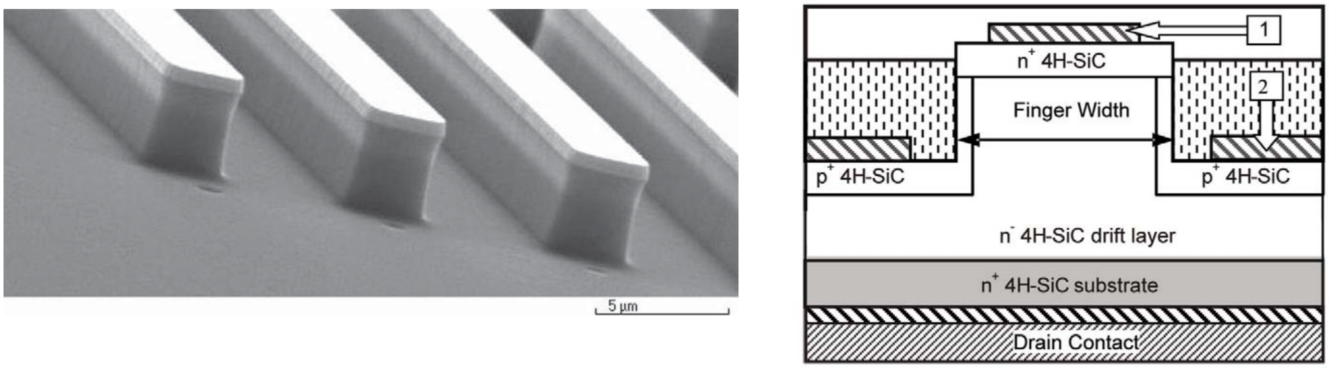

Fig. 2 (Left) A scanning electron micrograph (SEM) of a part-fabricated SiC vertical JFET device and schematic cross section (right). The SEM image shows the etched SiC fingers with Ni top electrode prior to ion implantation of the p-type layer and the gate contact. Note that the device is constructed from multiple fingers etched into the wafer surface.

well as a monolithically merged low-voltage, normally-off LJFET with high-voltage, normally-on VJFET (planar VJFET or P-VJFET)[28–30]. A purely vertical structure provides a good compromise between high current handling and high blocking voltage capabilities[2]. From the processing point of view, this structure enables a relatively simpler fabrication in that the vertical *pn*-junction may be formed by ion implantation instead of epitaxial regrowth on patterned substrates. The gate regions of these devices are typically fabricated either by deep implantation with ion energies in the range of several mega-electron-volts (DI-VJFET)[27,31] or by etching of trenches followed by implantation at relatively low ion energies in the range of several hundred kilo-electron-volts (TI-VJFET)[2,28,32–35]. Much progress has been made in the development of both normally-on[2,36] and normally-off high-power TI-VJFETs. Depending on the thickness of the n^- drift layer (W_D), such devices have been shown to be capable of blocking voltages up to 14 kV (at W_D = 115 μm)[37] – almost approaching the conventional theoretical limit of specific on-resistivity (R_{ON-S})[24]. At the same time, high-temperature operation of SiC VJFETs, which is necessary for a wide range of applications, remains barely addressed. Up to now, only SiC VJFETs operating at 150°C with a 40% drop in drain current density[30] and normally-on TI-VJFETs operating at junction temperatures up to 300°C with a fall of 30% from room temperature drain current values[36] have been reported.

Of the major classes of power semiconductor, the MOSFET probably has the greatest strategic importance in SiC power electronics, largely because it may offer majority-carrier operation and low gate current at voltage ratings approaching 5 kV. Although many devices have been demonstrated on 4H-SiC (see for example[38,39]), the measured on-state performance has been rather disappointing, largely because of the relatively poor effective channel mobility. Recently, however, devices fabricated using oxynitride techniques and on the carbon-face of the SiC crystal have yielded some particularly impressive results. A further complicating factor is that the field in the SiC must be limited to ~1 MVcm^{-1} to avoid excessive electric fields in the oxide. This necessitates suboptimal choices of epilayer doping and thickness. Buried-channel or depletion-mode devices[40,41] are attractive because they move the high field away from the SiC/SiO_x interface, resulting in reduced surface field and an improved lifetime. The material of choice for MOSFETs fabricated on the Si face appears to be 6H, but recent results for transistors fabricated on the $(11\bar{2}0)$ surface have shown encouragingly higher mobility for both 4H and 6H[42].

SiC offers the potential to fabricate double injected bipolar devices, such as the P-i-N diode or thyristor, with blocking voltages exceeding 25 kV using thick, lightly doped epilayers with long carrier lifetimes. At present, SiC growth technology does not yield lightly doped substrates and epitaxial layers are limited to less than ~100 μm in thickness with measured high-level lifetimes at best ~5 μS[43]. This places an upper limit of ~20 kV on the voltage blocking capability of any practical device. Further limitations arise from the built-in junction voltage drop, which is an unavoidable feature of any bipolar device and is ~2.8 V for SiC compared with around 0.7 V in Si. In addition, MOS-gated structures, such as the insulated gate bipolar transistor (IGBT), will only be effective if the epilayer resistance dominates the on-resistance of the equivalent MOSFET structure. With current SiC MOS technology, a 4H-SiC IGBT would only be effective at voltage blocking levels exceeding 4 kV (in Si, IGBTs become effective at ~300 V). Finally, the presence of deep levels, associated with common *p*-type dopants such as Al and B, gives cause for concern about the integrity of voltage blocking structures under dynamic conditions. This places an upper limit on the reverse *dv/dt* that can be applied without generating a dynamic punch-through condition[44].

In spite of these drawbacks, some impressive results have been reported for more conventional forms of bipolar power semiconductor. P-i-N diodes have been demonstrated with blocking voltages exceeding 10 kV and a current[45] of 20 A and with die areas up to 40 mm^2 and current ratings of up to 40 A for inclusion in 2.5 kV power modules alongside Si IGBTs[46]. Recently, some very promising results have been reported for BJTs[47]. These devices exhibit a relatively high current gain (–20), and an effective on-resistance of just 0.8 $\mathrm{m\Omega cm}^2$ (the lowest of any SiC power switch reported thus far) with a positive temperature coefficient. Note that the BJT structure does not suffer from the high forward voltage drop of other bipolar devices. Both conventional and gate turn-off (GTO) thyristors have been demonstrated at voltage levels between 400 V and 2.6 kV[48,49], and recently a *p*-channel IGBT has been fabricated[50,51]. There has also been considerable interest in high-voltage Schottky diodes as these offer very low stored charge – a great advantage for many power switching circuits. Schottky diodes with ratings up to 6 kV and operable at temperatures up to 500°C have been reported (Fig. 3)[52].

Fig. 3 Packaged SiC Schottky diodes.

SiC sensors

The excellent mechanical properties of SiC coupled to the high temperature stability of the material offer new possibilities for developing MEMS devices for more challenging applications than those possible with Si devices[53,54]. The need for a suitable etch-release layer (such as SiO_2) to make, for example, free-standing vibrating pressure sensors[55,56] requires different crystal growth capabilities than used for SiC electronic devices and it is the development of this growth technology that has, in many ways, determined the rate of progress of SiC MEMS technology. The dominant approach is the growth of 3C-SiC layers on either oxidized or nonoxidized Si wafers, as this clearly offers a route to larger wafer sizes than currently available for bulk SiC[57–61]. Of particular importance is the restriction of residual stresses that exist after growth of the 3C-SiC layers because high levels of residual stress reduce the signal-to-noise ratio in subsequently fabricated devices. The use of ultrahigh vacuum (UHV) CVD has proved fruitful here as it enables low-temperature growth (at or below 900°C), which markedly lowers residual stress[62]. The promise of surface micromachined SiC MEMS has led to similar processing capabilities to that of polycrystalline Si in terms of device sophistication[63]. An example of the typical level of achievement is shown in Fig. 4 where low-pressure (LP) CVD growth of 3C-SiC on Si (incorporating *in situ* doping during growth) has been used to produce excellent pressure sensor structures[64].

Another potential type of SiC sensor is the gas detector, typically based on a capacitor (metal-insulator-semiconductor or MIS structure) with a catalytic contact (Fig. 5)[65]. The dielectric layer allows these devices to operate at temperatures in excess of 900°C by separating the metal from the SiC[66]. The sensors function by a relatively simple mechanism – incoming hydrocarbon gases are decomposed by the catalytic metal, which generates both hydrogen and a range of gas fragments. These hydrogen and other hydrogen-containing molecules are further decomposed creating hydrogen atoms, which can diffuse easily through thick or dense catalytic contacts to form a charged layer in the dielectric. Decomposition of the gas molecules occurs at temperatures above 150°C in the submillisecond time scale[67]. The hydrogen atoms bond to the structure of the dielectric creating a charged layer close the semiconductor surface, modifying the electrical properties of the device and allowing detection. The high response speed of such systems makes SiC sensors suitable for the detection of gas species in rapidly varying environments, such as close to the manifold region in car exhausts[68], unlike conventional ceramic-based sensors that have a response time of ~10 s under these conditions[69].

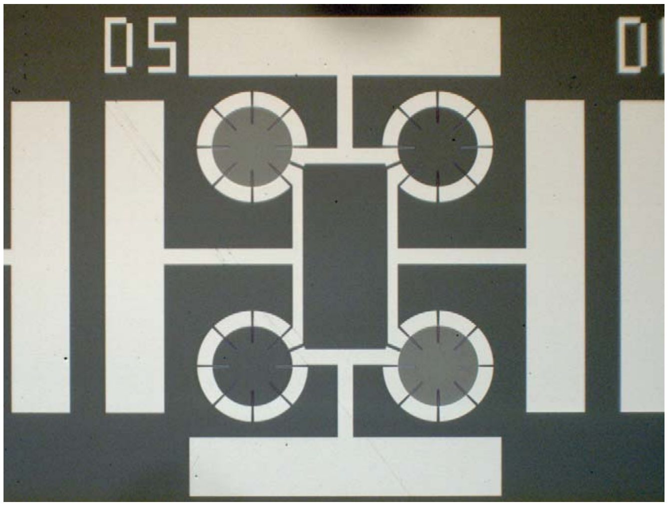

Fig. 4 An SEM image of a SiC pressure sensor.

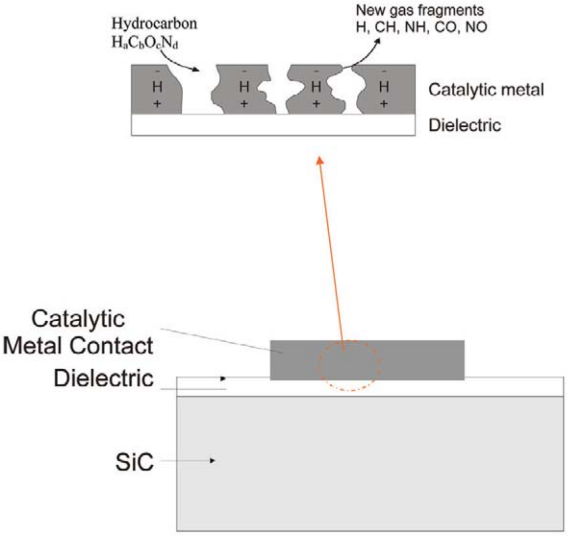

Fig. 5 Schematic cross section of a capacitive gas sensor (bottom). The top part shows a detailed cross section of the catalytic process that causes the gas to decompose and react. Incoming hydrocarbon gases break up into new fragments leaving a hydrogen-containing charged layer within the dielectric. This charged layer alters the electrical properties of the device and enables detection.

Despite having an indirect bandgap, a commercial ultraviolet (UV) photodetector using SiC has been demonstrated[70]. In comparison with other wide-bandgap optoelectronic materials, such as GaN, the major advantage is in the commercial availability of native substrates[71], which allows the fabrication of vertical detector structures, a lower defect density, and a more mature process technology[72]. The wide bandgap gives a lower intrinsic carrier concentration (a factor of 10^{18} less than for Si), which theoretically gives a far reduced dark current. However, at the current time, the high defect concentration in SiC makes the achievable dark current substantially higher than this[73].

Discussions and conclusions

We have reviewed the major types of electronic devices using SiC technology that have been proposed and discussed the major classes of application that may be envisaged. It is clear that there are many promising opportunities for SiC electronics and that we should be confident of future progress. The discussion has concentrated on relatively simple electronic and sensor devices, but it should be noted that there is considerable potential in more complex multi-quantum-well structures created from stacking different polytypes in thin layers – provided that difficulties such as antiphase boundary formation can be overcome. It is also interesting to note that sensor technologies may be less cost sensitive than other potential application areas for SiC devices, such as power electronic devices requiring large device areas. Typically, SiC sensors require small areas and are fabricated from either low-cost polycrystalline SiC on Si (in the case of many MEMS designs) or from relatively simple epitaxial layers on bulk SiC wafers. Thus, SiC sensors are generally less sensitive to the relatively high cost of SiC as a material – reducing one of the main barriers to the commercialization of SiC electronics.

Reduced cost concerns and potential system-level advantages are likely to ensure that many of the early commercial applications of SiC technology will be in the sensor domain. SiC sensor technology may become the dominant device technology, while larger markets in SiC power electronic devices are developed. The cost premium for SiC devices in comparison with those fabricated from traditional semiconductor materials, such as Si, will limit the deployment of these devices to markets where the material properties offer a unique advantage. The commercial prospects of SiC electronics are thus both enabled and also limited by material issues.

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